REMARKS/ARGUMENTS

Claims 9-18 are pending. Claims 9-15 and 17 are rejected under 35 USC 103(a), and claims 16 and 18 are indicated as allowable if rewritten in independent form including all the limitations of the base claim and any intervening claims.

Claims 9, 10, 14, and 16-18 have generally been amended to correct inadvertent errors and to more clearly set forth the invention. Claim 15 has been canceled.

Claim rejections under 35 USC 103(a)

Claims 9-15 and 17 were rejected under 35 USC 103(a) as being unpatentable over USPN 6,046,487 to Benedict et al. ("Benedict") alone or over Benedict in view of USPN 4,774,556 to Fujii et al. ("Fujii). These rejections are respectfully traversed.

Claim 9 has been amended to move the language "forming a gate dielectric layer" from the preamble to the body of the claim. This claim limitation is nowhere taught or suggested by Benedict because Benedict is directed to an isolation trench which is completely filled with insulating material. Thus, the isolation trench does not include a gate and as a result can not include a "gate dielectric layer." In contrast, Applicants' claim 9 is directed to forming "a trench field-effect transistor" including the step of forming "a gate dielectric layer inside the trench." Thus, Benedict fails to teach or suggest "forming a gate dielectric layer inside the trench" as recited in Applicants' claim 9.

Any reliance on the teachings of Fujii to overcome this deficiency of Benedict would be improper because no motivation can be found for combining these two references. The Examiner indicates that it would have been obvious to combine the conductive gate in Figs. 15 and 16 of Fujii with the dielectric layers in Fig. 2E of Benedict "to obtain a trench transistor type having small scale structure." But, Benedict nowhere states or even suggests that use of dielectric layers 42, 18, 44 (Fig. 2E) helps in any way to obtain a smaller scale structure. Nor is there any suggestion in Benedict that the dielectric layers 42, 18, 44 (Fig. 2E) have any use in non-volatile memory devices.

Claim 9 further distinguishes over Benedict by reciting:

> "heating the substrate to at least about 1,100°C to form a first layer of silicon oxide at least about 100Å thick inside the trench"

The Examiner concedes that Benedict fails to disclose the above cited step of Applicants' claim 9, and then attempts to overcome this deficiency in Benedict by stating:

> "The heating temperature of the substrate at 1,100 C degrees is considered to involve routine optimization while has been held to be within the level of ordinary skill in the art, [a]s noted In re Aller 105 USPQ 233, 255 CCPA 1955. [T]he selection of reaction parameters such as concentration and temperature would have been obvious."

This is respectfully traversed because as explained below, Applicants' step of forming a first layer of silicon dioxide inside a trench of a trench filed-effect transistor at a temperature of at least 1,100°C is contrary to accepted wisdom in the art, and thus is non-obvious (see MPEP 2145,X,D,3).

At page 3, lines 4-6 of the specification, Applicants make clear that "the lower temperatures (e.g., 950°C) [were] conventionally used in the industry" in forming the gate oxide layer in trench transistors. The Applicants at page 6, lines 22-27 of the specification further provide:

> "The present invention achieves this, in one embodiment, by growing the oxide layer at a temperature well above the temperatures used in conventional thermal oxidation processes. For example, conventional thermal oxide processes take place at about 900-950 °C. At this temperature, a thin oxide of a few hundred Angstroms can be grown in a controllable amount of time, such as several minutes."

At page 7, lines 7-12 of the specification, the Applicants identify known problems that arise in using elevated temperatures in forming the silicon dioxide layer:

> "At such elevated temperatures, limited thermal budgets and rapid oxide growth can become problems if steps are not taken to address these effects."

Thus, Applicants make clear that the conventional wisdom in forming a silicon dioxide layer was to use temperatures in the range of 900-950°C because of such issues as the limited thermal budget and rapid oxide growth that arise if higher temperatures were used. However, the Applicants have discovered that a significantly higher temperature used in forming

the silicon dioxide layer results in "substantially reduced corner thinning and substantially reduced residual stress at the corners" of the trench (page 6, line 29 to page 7, line 1). The applicants addressed the issues that arise in using high temperatures by using rapid thermal processing (RTP) "to avoid exceeding the thermal budget allowed by the process flow" (page 7, lines 9-10), and by reducing the "partial pressure of oxygen in the furnace in order "to slow down oxide growth" (page 7, lines 11-12 of the specification).

Section 2145,X,D,3 of the MPEP in part provides:

> "The totality of the prior art must be considered, and proceeding contrary to accepted wisdom in the art is evidence of nonobviousness. In re Hedges, 783 F.2d 1038, 228 USPQ 685 (Fed. Cir. 1986) (Applicant's claimed process for sulfonating diphenyl sulfone at a temperature above 127°C was contrary to accepted wisdom because the prior art as a whole suggested using lower temperatures for optimum results as evidenced by charring, decomposition, or reduced yields at higher temperatures)."

As in In re Hedges, Applicants' claimed process for forming the silicon dioxide layer inside the trench of a trench field-effect transistor at temperatures well above the 900-950°C was contrary to the accepted wisdom because, as indicated by the Applicants, conventional methods suggested using lower temperatures for optimum results as evidenced by the excessive loss of the thermal budget and the undesirable rapid oxide growth at higher temperatures.

Therefore, because using a high temperature of at least 1,100°C in forming a layer of silicon dioxide in the trench of a trench field-effect transistor is contrary to accepted wisdom in the art, such step would be non-obvious.

Claim 9 and its dependent claims 10-13 and 17-18 thus distinguish over the cited references for at least the above-stated reasons.

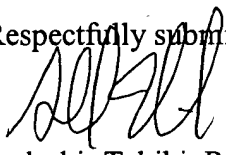
Independent claim 14 includes similar limitations to those of claim 9 cited above, and thus claim 14 and its dependent claim 16 distinguish over the cited references at least for the same reasons as claim 9 stated above.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,



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